REMARKS

Applicants note that new claims 44-59 were added in the previous Response mailed on September 9, 2005. No new matter was added. Support for the new claims is found in at least Figure 3 and the associated discussion in the present application. Thus, claims 1-12 and 44-59 are pending in the present application. The Examiner provided no indication in the present Office Action that the new claims have been entered and so, for the Examiner's convenience, Applicants have re-submitted the claim amendments that were presented in the previous Response, as indicated above.

In the Office Action, claims 1-2, 4-8, and 10-12 were rejected under 35 U.S.C. § 102(b) as allegedly being anticipated by Nishihara, et al (U.S. Patent No. 5,286,673). Claim 3 was rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over Nishihara in view of Ridinger (U.S. Patent No. 4,724,219). Claim 9 was rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over Nishihara in view of Jang (U.S. Patent No. 6,049,137). The Examiner's rejections are respectfully traversed.

With regard to independent claim 1, Applicants describe and claim providing a wafer comprised of a bulk substrate, an insulating layer positioned above the bulk substrate, and a semiconducting layer positioned above the insulating layer. For example, Applicants describe forming a silicon-on-insulator (SOI) structure including a silicon substrate, a silicon dioxide insulating layer, and an epitaxial silicon semiconductor layer. See Patent Application, page 10, ll. 21-24 and Figure 1. Applicants further describe and claim forming an opening in the semiconducting layer and the insulating layer to thereby expose a surface area of the bulk substrate, and forming an alignment mark in the bulk substrate within the exposed surface area of

the bulk substrate. Applicants also describe and claim forming a layer of material above the alignment mark and in the opening.

Nishihara describes forming a silicon dioxide layer 2 over a silicon substrate 1 and forming an opening 9a in the silicon dioxide layer 2. See Nishihara, col. 4, ll. 5-10 and Figure 5(a). A conductive poly-silicon film is deposited over the entire surface of the silicon substrate 1 and then the conductive poly-silicon film is etched using a photoresist mask 7 to form an alignment marking electrode 3a in the opening 9a. See Nishihara, col. 4, ll. 11-20 and Figure 5(b). In rejecting independent claim 1, the Examiner has apparently equated the silicon substrate 1 with the bulk substrate, the silicon dioxide layer 2 with the insulating layer, and the conductive poly-silicon film with the silicon semiconductor layer. Applicants respectfully submit that equating these layers is incorrect because the poly-silicon film described in Nishihara is conductive and therefore is not a semiconductor layer.

Even if the Examiner's reasoning is accepted for the sake of argument, Nishihara still fails to describe or suggest all the limitations of independent claim 1. Nishihara describes forming an opening 9a in the silicon dioxide layer 2. However, Nishihara also teaches that the conductive poly-silicon film is etched using a photoresist mask 7 to form an alignment marking electrode 3a in the opening 9a. Thus, Nishihara fails to teach or suggest forming an opening in the conductive poly-silicon film. Furthermore, Nishihara teaches that the conductive poly-silicon film is deposited over the entire surface of the silicon substrate 1 and then the conductive poly-silicon film is etched to form the alignment marking electrode 3a. Thus, Nishihara fails to teach or suggest forming an alignment mark in the bulk substrate within the exposed surface area of the bulk substrate.

For at least the aforementioned reasons, Applicants respectfully submit that the present invention is not anticipated by Nishihara and request that the Examiner's rejections of claims 1-2, 4-8, and 10-12 under 35 U.S.C. 102(b) be withdrawn.

Moreover, it is respectfully submitted that the pending claims are not obvious in view of Nishihara, Ridinger, or Jang, either alone or in combination. To establish a *prima facie* case of obviousness, the prior art reference (or references when combined) must teach or suggest all the claim limitations. *In re Royka*, 490 F.2d 981, 180 U.S.P.Q. 580 (CCPA 1974). As discussed in detail above, Nishihara fails to teach or suggest forming a silicon-on-insulator (SOI) structure including a silicon substrate, a silicon dioxide insulating layer, and an epitaxial silicon semiconductor layer. Nishihara also fails to teach or suggest forming an opening in the semiconducting layer and the insulating layer to thereby expose a surface area of the bulk substrate. Nishihara further fails to teach or suggest forming an alignment mark in the bulk substrate within the exposed surface area of the bulk substrate.

Nishihara also fails to provide any suggestion or motivation to modify the prior art of record to arrive at Applicants claimed invention. To the contrary, Nishihara teaches away from the present invention in at least three respects. First, Nishihara teaches that a conductive poly-silicon film is deposited over the entire surface of the silicon substrate 1, which teaches away from forming a semiconducting layer above the insulating layer. Second, Nishihara teaches that the conductive poly-silicon film is etched to form the alignment marking electrode 3a, which teaches away from forming an opening in the semiconductor layer and the insulating layer. Third, Nishihara's combined teaching that the conductive poly-silicon film is deposited over the entire surface of the silicon substrate 1 and then the conductive poly-silicon film is etched to form the alignment marking electrode 3a teaches away from forming an alignment mark in the

bulk substrate within the exposed surface area of the bulk substrate. It is by now well established that teaching away by the prior art constitutes *prima facie* evidence that the claimed invention is not obvious. *See, inter alia, In re Fine,* 5 U.S.P.Q.2d (BNA) 1596, 1599 (Fed. Cir. 1988); *In re Nielson,* 2 U.S.P.Q.2d (BNA) 1525, 1528 (Fed. Cir. 1987); *In re Hedges,* 228 U.S.P.Q. (BNA) 685, 687 (Fed. Cir. 1986).

With particular regard to claim 3, the Examiner relies on Ridinger to teach a wafer diameter in a range of 3 to 6 inches. However, Ridinger does not remedy the aforementioned deficiencies of the primary reference. Thus, Applicants respectfully submit that claim 3 is not obvious over Nishihara in view of Ridinger and request that the Examiner's rejection of claim 3 be withdrawn.

With particular regard to claim 9, the Examiner relies on Jang to teach positioning a wafer in a photolithography stepper tool and reflecting light off and alignment mark. However, Jang does not remedy the aforementioned deficiencies of the primary reference. Thus, Applicants respectfully submit that claim 9 is not obvious over Nishihara in view of Jang and request that the Examiner's rejection of claim 9 be withdrawn.

With regard to the new claims 44-59, Applicants respectfully submit that claims 44-46 depend from independent claim 1 and are therefore are allowable over the cited prior art for at least the aforementioned reasons. With particular regard to new independent claim 47, Applicants describe and claim providing a wafer comprised of a bulk substrate, an insulating layer positioned above the bulk substrate, and a semiconducting layer positioned above the insulating layer. Applicants also describe and claim forming an opening in the semiconducting layer and the insulating layer to thereby expose an unpatterned surface area of the bulk substrate, forming an alignment mark in the bulk substrate within the exposed unpatterned surface area of

the bulk substrate, and forming a layer of material above the alignment mark and in the opening. Thus, for at least the aforementioned reasons, Applicants respectfully submit that claims 47-59 are allowable over the cited prior art.

For at least the aforementioned reasons, it is respectfully submitted that all claims pending in the present application are in condition for allowance. The Examiner is invited to contact the undersigned at (713) 934-4052 with any questions, comments or suggestions relating to the referenced patent application.

Respectfully submitted,

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Mark W. Sincell, Ph.D.
Reg. No. 52,226
Williams Morgan & Amerson, P.C.
10333 Richmond Avenue, Suite 1100
Houston, TX 77042
(713) 934-7000
(713) 934-7011 (Fax)

AGENT FOR APPLICANTS